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(54) Control circuit for display panel

(57) For image data of each display cell, correction is performed with data from a correction memory (12) and stored in an image memory (14). A sequencer sends a signal regarding a display pulse within one frame to a sequence counter (22), which the sequence counter counts. A value corresponding to the count value is read out from a look up table (24), and a comparator compares the image data for one display cell from the image memory with a value (number of discharges or value corresponding to brightness) regarding the display pulse converted from the lookup table (24). When the value from the lookup table (24) reaches the value of the image data, the display data is changed so as to control the state of discharge (such as to stop the discharge). The number of discharges corresponding to the image data is controlled by the contents of the lookup table (24) so that the brightness can be controlled and correction is easily performed.

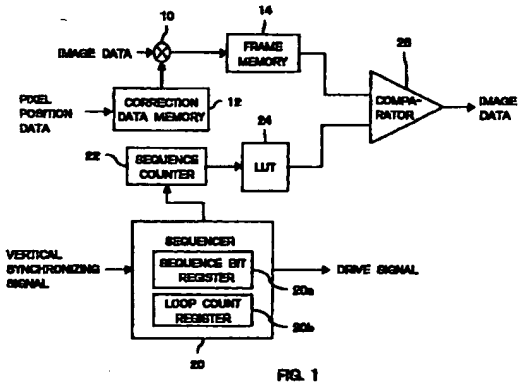

FIG. 1

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] This invention relates to a drive circuit for a display panel, disposed with a common electrode and an individual electrode in each of a plurality of display cells arranged in a matrix configuration, for controlling gas discharges in each display cell by applying display pulses to the common electrode to perform display operations and by individually applying control voltages to individual electrodes to control the discharge in each display cell.

2. Description of the Related Art

[0002] Heretofore, display panels, such as plasma displays, are known for performing display operations by controlling the gas discharge of every display cell. These types of display panels are formed by disposing display cells into many matrix configurations for individually performing gas discharges.

[0003] Usually, the discharges are performed in pulses and the number of discharges in one frame in each display cell is controlled by luminance information regarding the respective display cell. For example, through the luminance data that is input, the number of discharges is set to a maximum number when the luminance of the display cell is at maximum luminance, and the number of discharges is set to 0 at minimum luminance. Furthermore, one set of three types of RGB display cells form one pixel, and the driving of each display cell is controlled by individual RGB luminance data for one pixel.

[0004] When actually performing a display operation in the display panel, it is necessary to perform various types of correction, such as adjustment of tint or gamma correction for the luminance data. These types of correction were performed for luminance data in the same manner as the correction of ordinary image data.

[0005] The data processing for these types of correction usually use the same calculations. However, if a setting is to be changed, the calculation must also be changed. This change is difficult to accomplish if an attempt is made to implement the circuit in hardware. On the other hand, if the circuit is implemented in software, a lot of time is required and the load on the processor increases.

SUMMARY OF THE INVENTION

[0006] The object of this invention is to provide a display control circuit for a display panel that has simple circuitry using a lookup table and that performs high-speed processing.

[0007] The drive circuit for a display panel concerned with in this invention comprises a sequence counter for counting the number of display pulses to be supplied to the common electrode, a lookup table for outputting an assumed luminance value corresponding to and addressed by the count value of the sequence counter, and a comparator for comparing the assumed luminance data from the lookup table with luminance data that is input. An output of the comparator controls a period of applying control voltage to the individual electrode of one display cell. According to this apparatus, discharges can be controlled to occur or not occur by a control voltage to the individual electrode corresponding to a display pulse. Therefore, controlling the time of applying the control voltage to the individual electrode enables the number of discharges to be controlled and enables the luminance in the display cell to be controlled. Rewriting the contents of the lookup table enables the time of applying the control voltage to the individual electrode to be made to correspond to luminance data that is input so that the number of discharges can be controlled. Namely, the display becomes brighter with a larger number of discharges, so that by handling the data in the lookup table, the number of discharges, which changes with single units (one step) of luminance data, can be varied when the luminance data is small or when it is large. Therefore, various types of corrections, such as gamma correction, can be performed using the contents of the lookup table. Using the lookup table in this manner can speed up calculations and facilitate changes in characteristics. Having separate lookup tables to correspond with the RGB colors enables the individual brightness of the respective RGB color to be adjusted and also enables tint adjustments.

[0008] It is preferable for the above-mentioned lookup table to store differential data and to sequentially add the differential data that is output on the basis of the count value of the sequence counter so as to yield an assumed luminance value. This enables the same calculations to be performed with a narrower bit width of the lookup table.

[0009] It is also preferable to have a correction data table for storing correction data for each display cell so that the correction data corresponding to luminance data for each display cell that is input is read out from the correction data table for correction and the corrected luminance data is supplied to a comparator. This enables the adjustment of every display cell to be performed on the image data according to the correction data table, and the lookup table can store data for all display cells.

[0010] This invention is composed as described above and achieves the effects given below.

(i) The luminance of the display panel corresponding to the input luminance data is set by reading out the assumed luminance value from the lookup table according to the count value corresponding to the number of discharges, and by comparing this

assumed luminance value with the luminance data that is input. Thus, the luminance in the display cell corresponding to the luminance data that is input can be changed by rewriting the contents of the lookup table.

(ii) The same calculations can be performed with a narrower bit width of the above-mentioned lookup table by storing differential data into the lookup table.

(iii) By providing a correction data table for storing correction data for each display cell and by performing correction for the luminance data of each display cell that is input, the adjustment of every display cell can be performed on the image data according to the correction data table, and for using the lookup table, it does not matter to which display cell the data corresponds.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]

Fig. 1 is a block diagram showing a structure of one embodiment of this invention.

Fig. 2 shows the correction of light emission amount.

Fig. 3 shows a structure of a lookup table.

Fig. 4 shows a structure of a sequence bit register and a loop count register.

Fig. 5 shows a sequence operation.

Fig. 6 shows a discharge sequence.

Fig. 7 is a flowchart showing insertion of an insertion sequence.

Fig. 8 shows the insertion of a reset pulse in a stable state.

Fig. 9 shows a discharge state in the stable state.

Fig. 10 shows the insertion of the reset pulse in an unstable state.

Fig. 11 shows a discharge state in the unstable state.

Fig. 12 shows a structure of a display cell.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0012] One embodiment of this invention will be described hereinafter with reference to the attached drawings. Fig. 1 is a block diagram showing a structure of a display control circuit for a display panel of the embodiment.

[0013] Image data, which is RGB digital data for every pixel, is input by a multiplier 10. In the display panel, one pixel comprises three RGB display cells. One RGB data item at a time causes the discharge of the corresponding display cell to be controlled. The description below is based on the case where a single luminance data is input.

[0014] Correction data is supplied to the multiplier 10 from a correction memory 12, and correction is performed from the multiplication of the image data and correction data. The correction memory 12 stores correction data for every display cell. The correction data corresponding to the image data is read from the correction memory 12 and multiplied on the basis of the image position data that is input to yield error-corrected image data for every cell. This allows variations in luminance of the display cells to be corrected. It should be noted that the corrections need not necessarily be performed by multiplication but may be performed by the addition of differential data. In this embodiment, the image data has 9 bits and the correction data has 8 bits. With a "1" added to the most significant bit of the correction data for a total of 9 bits, 9×9 multiplication is performed and the most significant 9 bits are output from the multiplier 10 as the calculation result.

[0015] The corrected image data, which is the output of the multiplier 10, is stored in an image memory 14. The image data for at least one frame is stored in the image memory 14. Usually, the image data for one frame at a time is stored for R, G, and B, respectively.

[0016] In the meantime, a sequencer 20 generates and outputs a drive signal for common electrode drive after detecting the start of one frame with a vertical synchronizing signal. The display pulse is repeated in periods of one frame and supplied to the common electrode. The sequencer 20 then supplies a pulse signal, which is synchronized to the display pulse, to a sequence counter 22. Thus, a count value in the sequence counter 22 is determined by the number of display pulse outputs. The luminance of the display cell corresponds to the number of discharges in one frame. Since the number of discharges corresponds to the number of display pulses, the count value becomes the assumed luminance (assumed luminance data) when light is emitted due to the display pulses.

[0017] The output of the sequence counter 22 is supplied to a lookup table (LUT) 24. A predetermined conversion is performed according to this lookup table 24 and the converted assumed luminance data is input by a comparator 26. The image data from the image memory 14 is input to another input terminal of this comparator 26. A one-bit signal is then obtained from the comparator 26 in order to control the supply of the control voltage to the individual electrode of the display cell.

[0018] One data item is output from the lookup table 24 for each display cell in the display of one frame display. For a color display, there are three types of RGB data for one display unit (pixel: three types (RGB) of data for one pixel) so the image data for one frame (three types of RGB data for three frame memories) is output in parallel from the image memory 14. The comparator 26 is provided for each color, and at each comparator 26, the image data for each display cell and the assumed luminance data from the lookup table 24 are compared. The comparison results are individually output from the comparators 26 one by one as display data

of each display cell. Controlling the voltage applied to each individual electrode of each display cell by one frame of pixels x 3 (RGB) items of display data controls the light emission in each display cell so that a display on the display panel is performed.

[0019] For example, if the image data has 256 gradations and the number of pulses to be output from the sequencer 20 is 256 pulses, it is sufficient to cause the display cell to emit light by performing the discharge according to the display pulses until the output value of the sequence counter 22 is the same as the gradations of the image data. When the values that are input are identical at the comparator 26, it is sufficient to change the value of the display data and at this time to control the control voltage to be applied to the individual electrode so that the light emission ceases. In this embodiment, an arbitrary conversion can be performed for the assumed luminance data by means of the contents of the lookup table 24. Therefore, the light emission time can be set as desired in accordance with the gradations of the image data.

[0020] In this embodiment, the number of display pulse outputs in one frame is 765 pulses. If the lookup table 24 is set so that 0, 3, 6, 9, ..., 765 are output with respect to inputs 0, 1, 2, 3, ..., 255, one gradation corresponds to three discharges and both the input and output have a linear relationship.

[0021] In the meantime, if the amount of the increment or decrement is varied, such as if the value of the lookup table 24 is initially incremented by 1 and subsequently incremented by 5, the amount of light emission can be arbitrarily set according to the change in gradation as shown by the solid and broken lines in Fig. 2.

[0022] Thus, gamma correction can be achieved through the settings of the contents of the lookup table 24. Furthermore, through each of the RGB colors, the tint and so forth can be set by rewriting the contents of the lookup table 24.

[0023] By making it possible to rewrite the lookup table 24 in this manner, arbitrary characteristics can be set.

[0024] Fig. 3 shows an example of a structure of the lookup table 24. As shown, a 10-bit count value is supplied from the sequence counter 22. A table 24a has an organization of 4-bit x 1024 (although 765 is suitable if the maximum number of output display pulses is 765 as described above, 1024 is adopted since addressing is done with a 10-bit count value) and stores differential data for values to realize the characteristics shown in Fig. 2.

[0025] The output of the table 24a is supplied to an adder 24b. To this adder 24b is supplied data from a latch 24c and addition is performed. The output of the adder 24b is latched by the latch 24c. Therefore, the adder 24b sequentially adds its own previous output to the differential data from the table 24a, and an estimated value of the differential data is output from the adder 24b.

[0026] This sort of configuration enables 9-bit data to be output from the adder 24b with the table 24a having a 4-bit width. Therefore, the lookup table 24 can be small since 9-bit data need not be stored.

[0027] The operation of the sequencer will be described next. The sequencer 20 internally contains a sequence bit register 20a and a loop counter register 20b. Their structures are shown in Fig. 4.

[0028] The sequence bit register 20a stores the sequence for the drive signal and its period. Sequence bits B0 to B23 of each address A0 to A63 indicate values for output, and these values are, for example, commands for the drive voltage for the common electrode. Counter bits B0 to B7 indicate the output periods of the sequence bits. The counter bits can be, for example, the number of clocks of a system clock.

[0029] The loop count register 20b stores the address of the sequence bit register and the number of sequence outputs. Sequence address bits B0 to B4 of each address A0 to A63 indicate the address of the sequence bit register 20a, and the sequence output is performed according to this address setting. Furthermore, the counter bits B0 to B7 indicate the number of loops of the sequence to be performed at the specified address.

[0030] The operation at the sequencer 20 will be described here with reference to Fig. 5. The sequencer 20 first reads (S1) the top address A0 of the loop count register 20b. Next, the sequence bit of the sequence bit register 20a at the address specified by the sequence address of the loop count register is output for the period specified by the counter bit (S2). When the output of S2 terminates, the address of the sequence bit register 20a is incremented by 1 (A1 follows A0) (S3). It is then judged whether the count value of the sequence bit register 20a has been set to 0 (S4).

[0031] If the count value of the sequence register 20a is a specific value (in this case 0), the setting is made to signify the termination of the successive output of the sequence in the sequence register 20a.

[0032] If the result of the judgment in S4 is NO, the sequence bit of the next address (address in the previous process incremented by 1) of the sequence bit register 20a is output for the count period (S5). When this is terminated, the operation returns to S3, which increments the sequence bit register 20a by one. The output of the sequence stored in the sequence bit register 20a is repeated, and the output of the sequence in the sequence bit register 20a is repeated until the count value of the sequence bit register 20a reaches 0. A count value other than 0 signifies that some type of output is to be performed while a count value of 0 signifies that the output is not to be performed or the termination of the sequence.

[0033] Then, when the count value of the sequence bit register 20a becomes 0 and the result of S4 is YES, the operation returns to the loop count register 20b where it is judged whether the specified number of loops of the

count has been performed (S6). If the specified number of loops has not been performed, the operation returns to S2 where the sequence of the sequence bit register of the address specified by the loop count register 20b at the time is output.

[0034] In this manner, if the process specified by one address of the loop count register 20b terminates (termination of the specified number of loops of the count of the loop count register 20b) and the result of S6 is YES, the address of the loop count register 20b is incremented by 1 (S7). It is then judged whether the count value of the loop count register 20b is 0 (S8).

[0035] If the count value is 0, this signifies that the corresponding sequence is not to be performed. Therefore, not performing the output signifies the termination of the sequence so in this case the sequence is terminated. On the other hand, if the count value of the loop count register 20b is not 0, the operation returns to S2 and the sequence bit of the sequence bit register of the address specified by the loop count register 20b is output for the count period.

[0036] In this manner, the output of the common pulse to the common electrode is performed. Controlling the voltage of the individual electrode on the basis of the display data in the period in which the output of this common pulse is performed enables the light emission of each display cell to be controlled.

[0037] For example, as shown in Fig. 6, the display pulse in which the voltage from the common electrode rises and falls in two levels is repetitively output and the control voltage at the individual electrode is individually controlled. As a result, a discharge occurs when the control voltage at the individual electrode is set low, and the discharge is inhibited when the control voltage is changed to high. This achieves luminance control by controlling the light emission time or number of discharges.

[0038] Next, in addition to the synchronization sequence for synchronizing to the vertical synchronizing signal to be executed every time in each frame so that the display pulse is applied onto the common electrode as a sequence, the sequencer of this embodiment also contains an insertion sequence for inserting the reset pulse only into a predetermined frame. The execution of this insertion sequence is identical to the execution of the above-mentioned sequence except that the output differs.

[0039] This insertion sequence is inserted before the actual display (discharge due to display pulses) begins. This is described with reference to Fig. 7. It is first judged whether the vertical synchronizing signal has arrived (S11). Although this vertical synchronizing signal signifies the termination of the vertical retrace period, it may also signify the start or middle of the vertical retrace period.

[0040] The vertical synchronizing signal is counted (S12) when it arrives. This is then compared with the value stored in the register (S13). For example, if this sequence is to be performed every three frames, a "3" is stored in the register. Then, if the count is greater than or equal to the stored value of the register, the insertion sequence is performed (S14).

[0041] If the operation of the insertion sequence terminates or if the count value in S13 has not reached the value stored in the register, the synchronization sequence is performed (S15). As a result, according to the value stored in the register, the insertion sequence can be executed at every predetermined frame. It is preferable to execute this insertion sequence prior to the start of the synchronization sequence that is to be performed each time.

[0042] Changing the stored value in the register enables the timing for the execution of the insertion sequence to be arbitrarily set, and enables the insertion sequence to be executed as desired in the sequencer 20.

[0043] It is preferable to insert the reset pulse here as the insertion sequence. The reset pulse applies a negative voltage to the common electrode so that wall charges can be erased.

[0044] When the power is turned on, the discharge may not occur normally due to insufficient voltage and wall charges may collect in the display cell. The wall charges may remain even with continuous discharges. In this case, applying a reset pulse having a polarity opposite to that of the display pulse to the common electrode causes a discharge to erase any wall charges that are present so that subsequent discharges can be performed normally.

[0045] For example, when the reset pulse has been inserted as the insertion sequence, a negative reset pulse is inserted between display pulses as shown in Figs. 8 and 9. If a stable discharge occurred with the previous display pulse, the reset pulse does not cause a discharge. On the other hand, if an unstable discharge occurred with the previous display pulse as shown in Figs. 10 and 11, wall charges remain. Inserting a reset pulse then causes a discharge to erase the wall charges so that a stable discharge subsequently occurs. With regard to the insertion sequence, the execution method in the sequence 20 is identical to that for the above-mentioned synchronization sequence. The reset pulse should be inserted during the normal vertical synchronizing period or sometime prior to the start of the subsequent display.

[0046] Particularly, in this embodiment, the reset pulse was designed to have a polarity opposite to that of the display pulse. It is then simply a matter of controlling only the sequence for the driving of the common electrode, and this can be performed under control of the sequencer 20.

[0047] Furthermore, in this embodiment, a pulse having a polarity opposite to that of the display pulse is employed for the reset pulse, and is applied to the common electrode. This obviates the need to apply a separate voltage for wall charge erasure to the individual

electrode. Therefore, it is not necessary to apply high voltages in the drive circuit for the individual electrode and the frequency of applying voltages to the individual electrode can be low. Namely, when applying the pulse for initialization to the individual electrode to erase wall charges, a considerably high voltage is necessary, and the driving frequency for the individual electrode rises when this pulse is inserted for initialization. However, since the individual electrode changes state only once in one frame in this embodiment, the rise in driving frequency for the individual electrode can be suppressed.

[0048] Fig. 12 shows the structure of one display cell (one color) in a display panel of the embodiment. On a rear side of the display panel there is provided a back glass plate 30. On the inner surface of a recess 32 formed in the back glass plate 30 there is formed a fluorescent layer 34. On a rear side (side facing the back glass plate 30) of a front glass plate 40 there are disposed a pair of transparent electrodes 44a and 44b. A dielectric layer 46 is formed so as to cover them, and a protective film 48 is further formed. Therefore, the protective film 48, which is usually formed from MgO, faces the recess 32. A positive display pulse is applied to the common electrode and the individual electrode is maintained at a sufficiently low voltage (for example 0 V) so that a discharge occurs at a part close to the protective film within the recess 32. A positive voltage is applied to the individual electrode so that the voltage value between the individual electrode and common electrode drops and the discharge ceases to occur.

[0049] The control voltage in the individual electrode is controlled by the above-mentioned display data and the drive of the common electrode is controlled by the output from the sequencer 20.

[0050] While there has been described what are at present considered to be preferred embodiments of the invention, it will be understood that various modifications may be made thereto, and it is intended that the appended claims cover all such modifications as fall within the true spirit and scope of the invention.

Claims

1. A display control circuit for controlling, on the basis of luminance data that is input, a gas discharge of a display panel comprising an individual electrode disposed in each of a plurality of display cells disposed in a matrix configuration and a common electrode disposed in common with the plurality of display cells, comprising:

   - a sequence counter (22) for counting the number of display pulses to be supplied to the common electrode;
   - a lookup table (24) for outputting an assumed luminance value corresponding to the counted number of display pulses addressed by the count value of the sequence counter (22); and
   - a comparator (26) for comparing the assumed luminance data from the lookup table (24) with luminance data that is input,
   - wherein an output of the comparator (26) controls a period of applying control voltage to the individual electrode of one display cell.

2. The control circuit according to claim 1, wherein one such comparator (26) is provided to correspond to one display cell.

3. The control circuit according to claim 1 or 2, wherein the lookup table (24) has a content that can be rewritten.

4. The control circuit according to any of claims 1 to 3, wherein the lookup table (24) stores differential data and obtains an assumed luminance value by sequentially summing the differential data that is output according to the count value of the sequence counter (22).

5. The control circuit according to any of claims 1 to 4, comprising:

   - a correction data table (12) for storing correction data regarding each display cell,
   - wherein correction data corresponding to luminance data for each display cell that is input is read out from the correction data table (12) for correction and the corrected luminance data is supplied to a comparator (26).

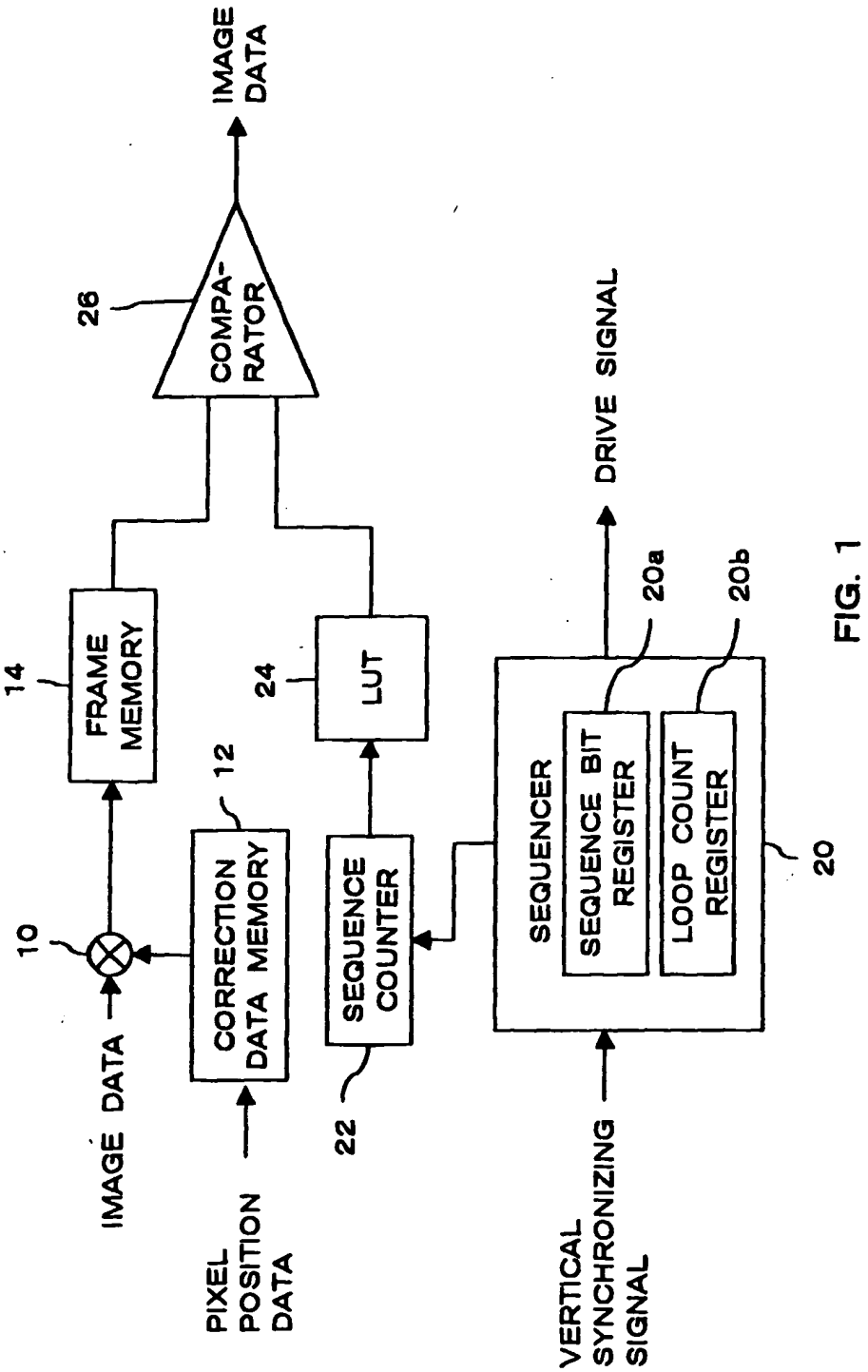
IMAGE DATA
26
COMPA-RATOR
DRIVE SIGNAL
14
FRAME MEMORY
24
LUT
20a
20b
12
10
CORRECTION DATA MEMORY
SEQUENCE COUNTER
SEQUENCER
SEQUENCE BIT REGISTER
LOOP COUNT REGISTER
20
IMAGE DATA
PIXEL POSITION DATA
22
VERTICAL SYNCHRONIZING SIGNAL

FIG. 1

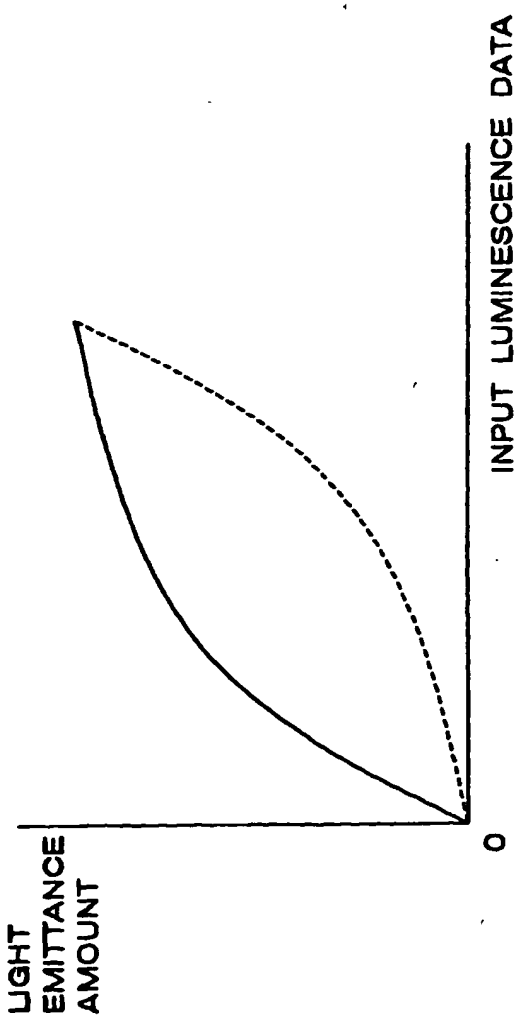

FIG. 2

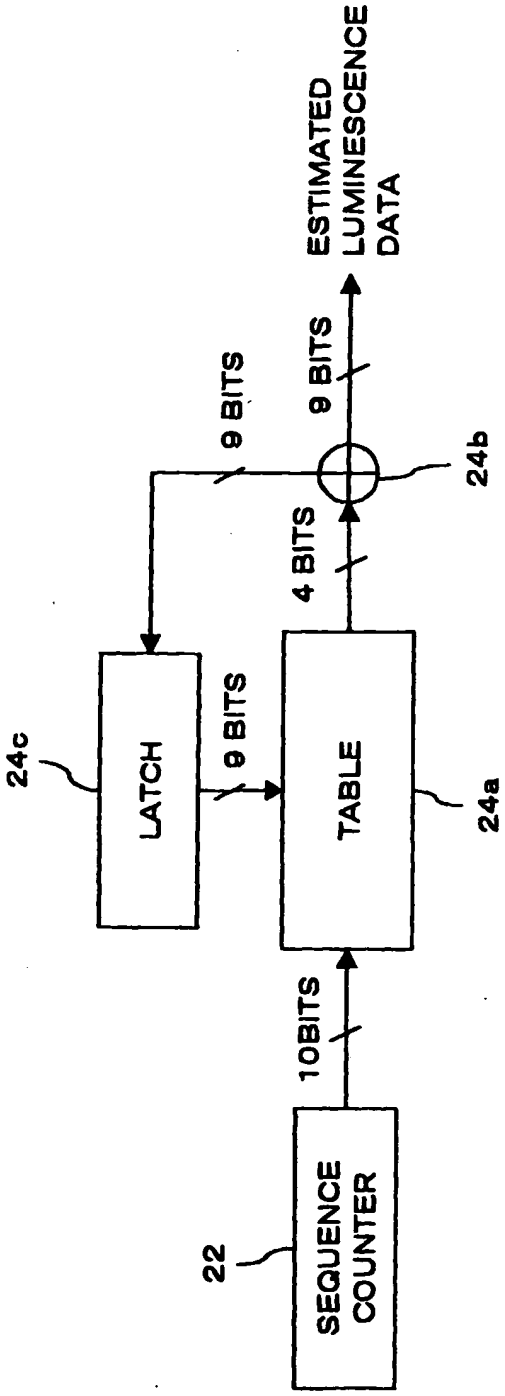
ESTIMATED LUMINESCENCE DATA
9 BITS
9 BITS
24b
4 BITS
24c
LATCH
9 BITS
TABLE
24a
10BITS
22
SEQUENCE COUNTER

FIG. 3

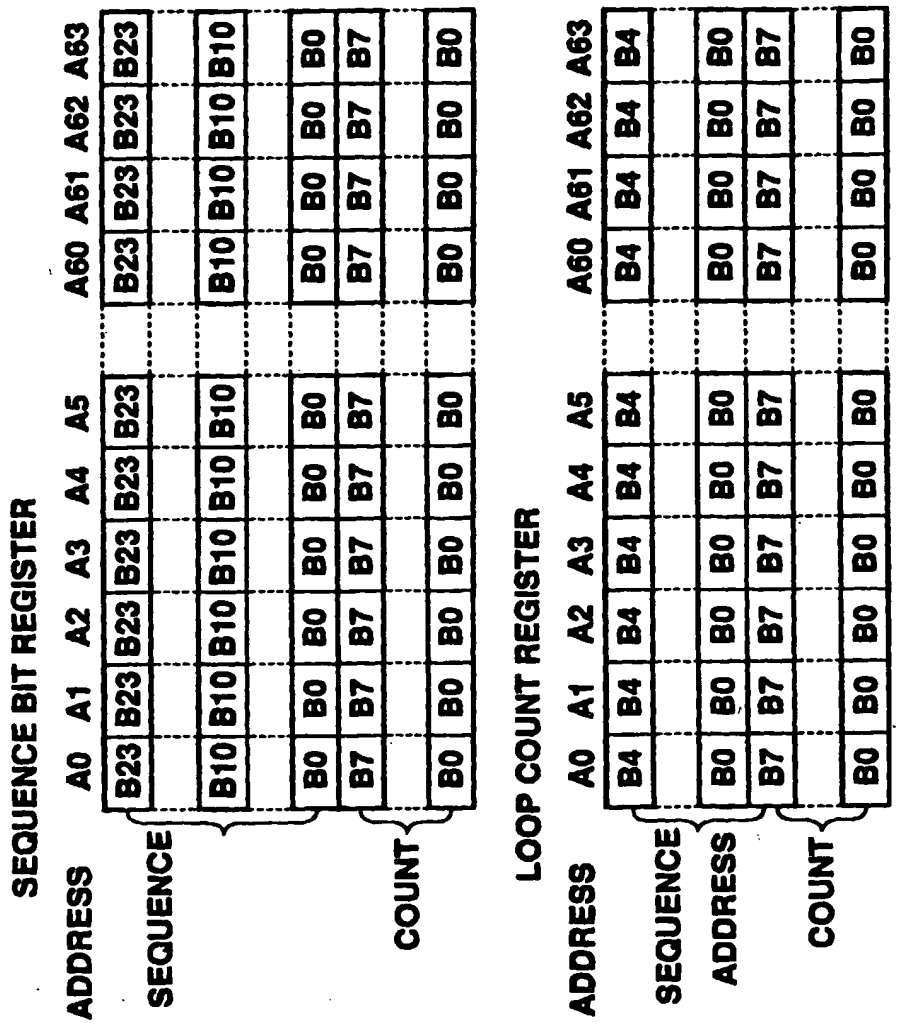
SEQUENCE BIT REGISTER
ADDRESS
SEQUENCE
COUNT
A0 A1 A2 A3 A4 A5 A60 A61 A62 A63
B23 B23 B23 B23 B23 B23 B23 B23 B23 B23
B10 B10 B10 B10 B10 B10 B10 B10 B10 B10
B0 B0 B0 B0 B0 B0 B0 B0 B0 B0
B7 B7 B7 B7 B7 B7 B7 B7 B7 B7
B0 B0 B0 B0 B0 B0 B0 B0 B0 B0
LOOP COUNT REGISTER
ADDRESS
SEQUENCE
ADDRESS
COUNT
A0 A1 A2 A3 A4 A5 A60 A61 A62 A63
B4 B4 B4 B4 B4 B4 B4 B4 B4 B4
B0 B0 B0 B0 B0 B0 B0 B0 B0 B0
B7 B7 B7 B7 B7 B7 B7 B7 B7 B7
B0 B0 B0 B0 B0 B0 B0 B0 B0 B0

Fig. 4

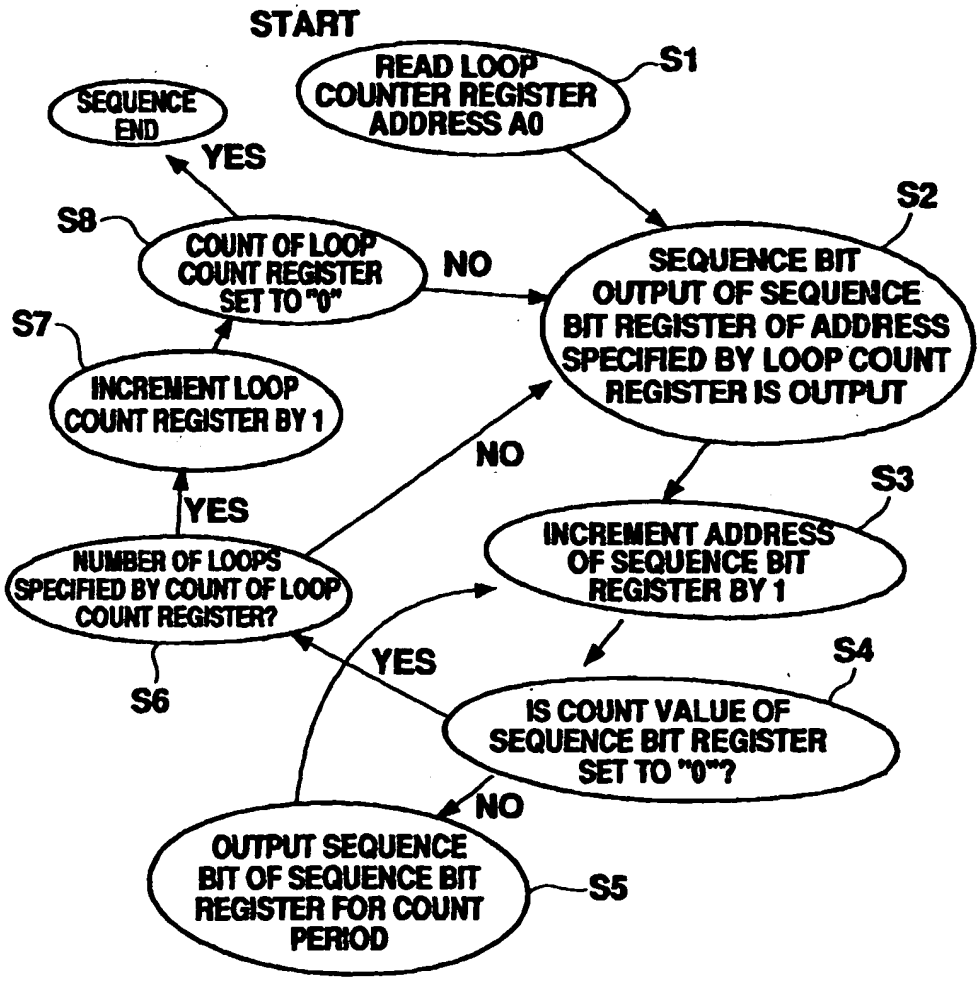
START
READ LOOP COUNTER REGISTER ADDRESS A0
S1
SEQUENCE BIT OUTPUT OF SEQUENCE BIT REGISTER OF ADDRESS SPECIFIED BY LOOP COUNT REGISTER IS OUTPUT
S2
INCREMENT ADDRESS OF SEQUENCE BIT REGISTER BY 1
S3
IS COUNT VALUE OF SEQUENCE BIT REGISTER SET TO "0"?
S4
OUTPUT SEQUENCE BIT OF SEQUENCE BIT REGISTER FOR COUNT PERIOD
S5
NUMBER OF LOOPS SPECIFIED BY COUNT OF LOOP COUNT REGISTER?
S6
INCREMENT LOOP COUNT REGISTER BY 1
S7
COUNT OF LOOP COUNT REGISTER SET TO "0"
S8
SEQUENCE END
YES
NO
YES
NO
YES
NO

Fig. 5

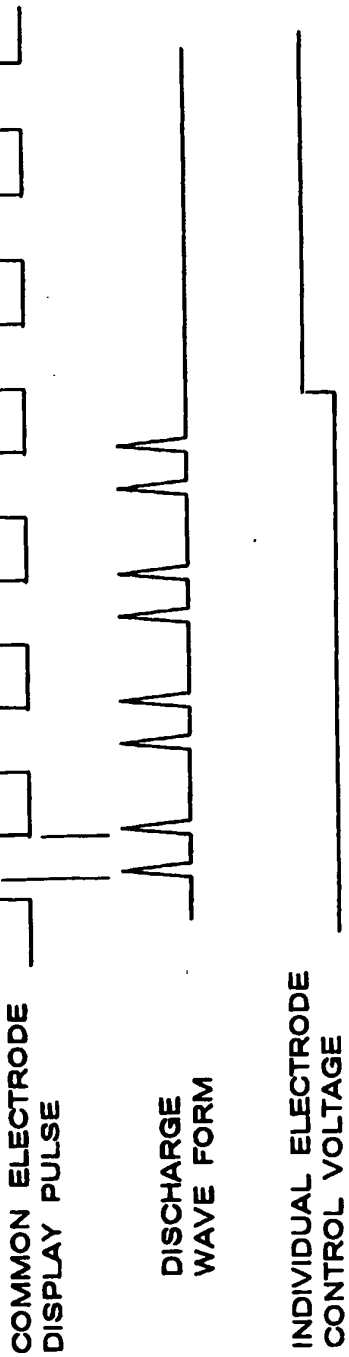
COMMON ELECTRODE
DISPLAY PULSE
DISCHARGE
WAVE FORM
INDIVIDUAL ELECTRODE
CONTROL VOLTAGE

FIG. 6

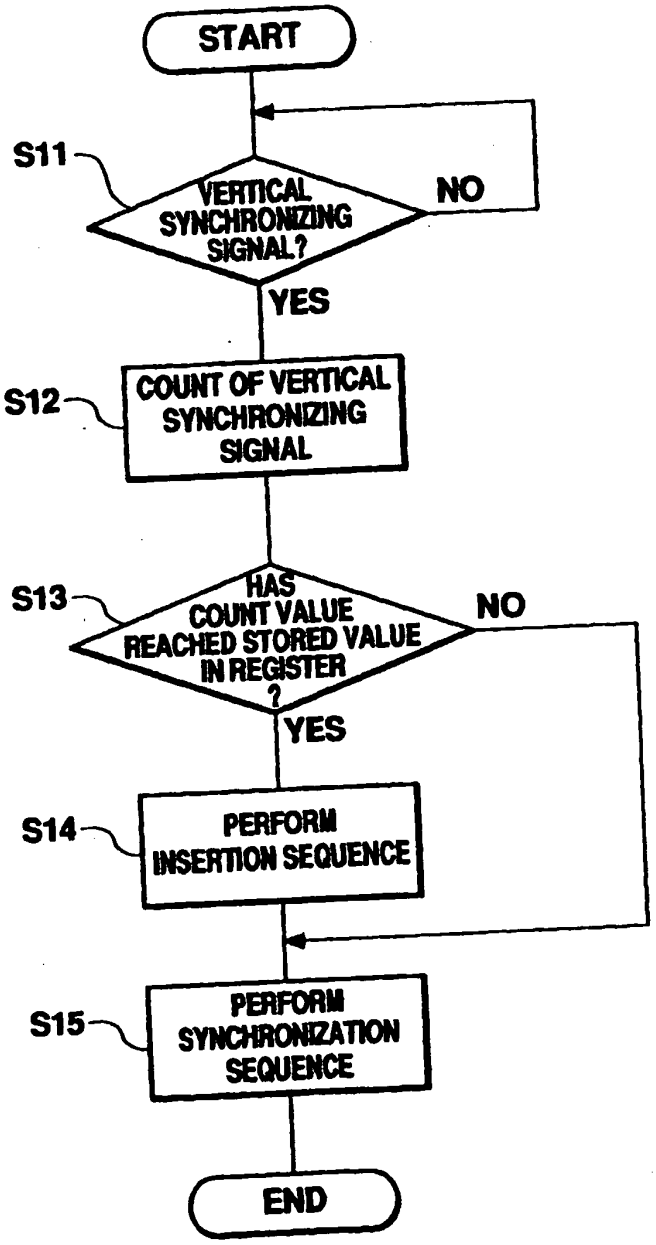
START
S11
VERTICAL SYNCHRONIZING SIGNAL?
NO
YES
S12
COUNT OF VERTICAL SYNCHRONIZING SIGNAL
S13
HAS COUNT VALUE REACHED STORED VALUE IN REGISTER ?
NO
YES
S14
PERFORM INSERTION SEQUENCE
S15
PERFORM SYNCHRONIZATION SEQUENCE
END

Fig. 7

DISPLAY PULSE
RESET PULSE
COMMON ELECTRODE DISPLAY PULSE
DISCHARGE WAVE FORM
INDIVIDUAL ELECTRODE CONTROL VOLTAGE

FIG. 8

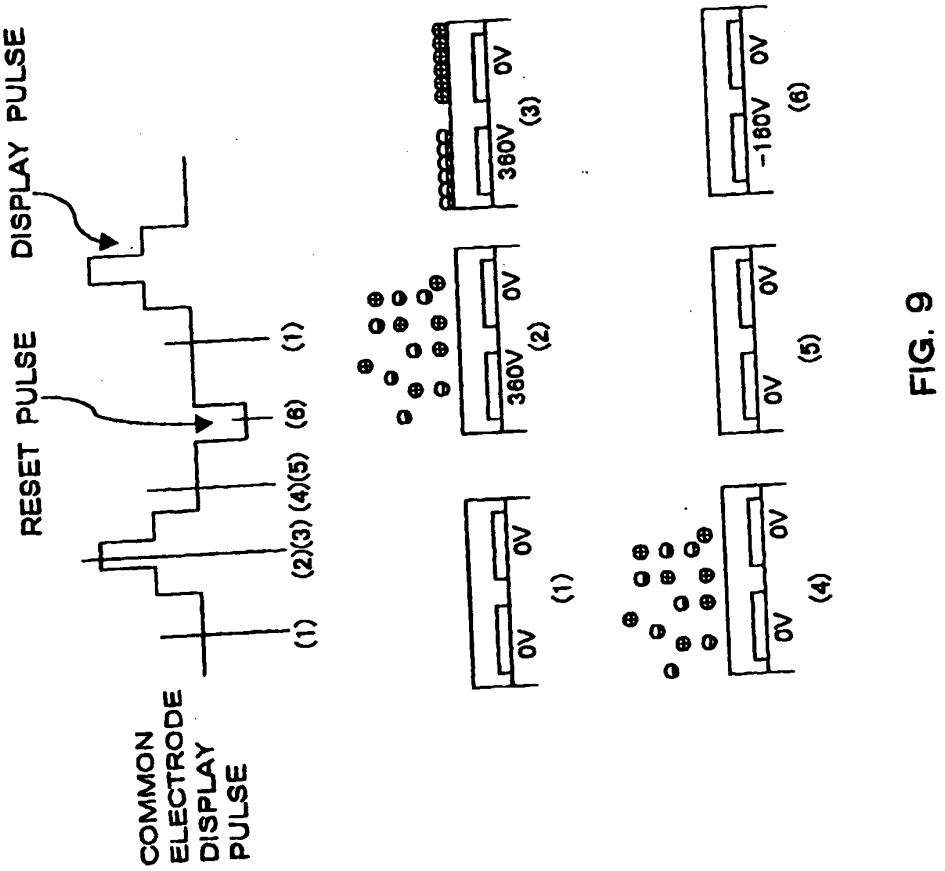
DISPLAY PULSE
RESET PULSE
COMMON ELECTRODE DISPLAY PULSE
(1)
(2)(3)
(4)(5)
(6)
(1)
0V
0V
(1)
360V
0V
(2)
360V
0V
(3)
0V
0V
(4)
0V
0V
(5)
-180V
0V
(6)

FIG. 9

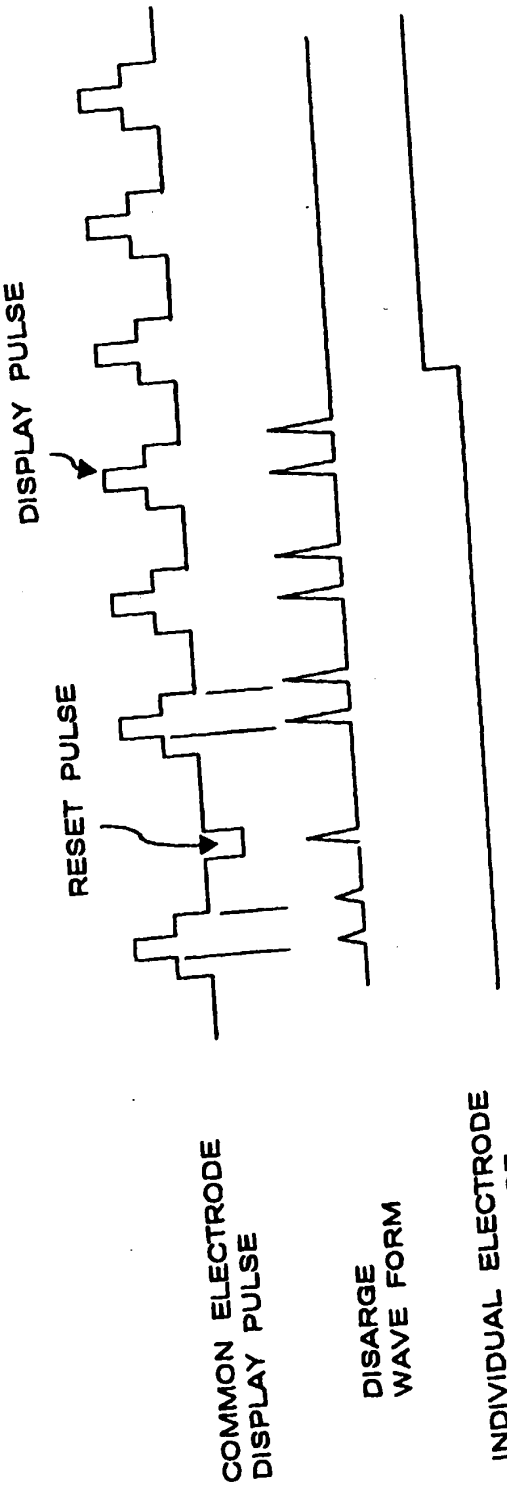
DISPLAY PULSE
RESET PULSE
COMMON ELECTRODE DISPLAY PULSE
DISARGE WAVE FORM
INDIVIDUAL ELECTRODE CONTROL VOLTAGE

FIG. 10

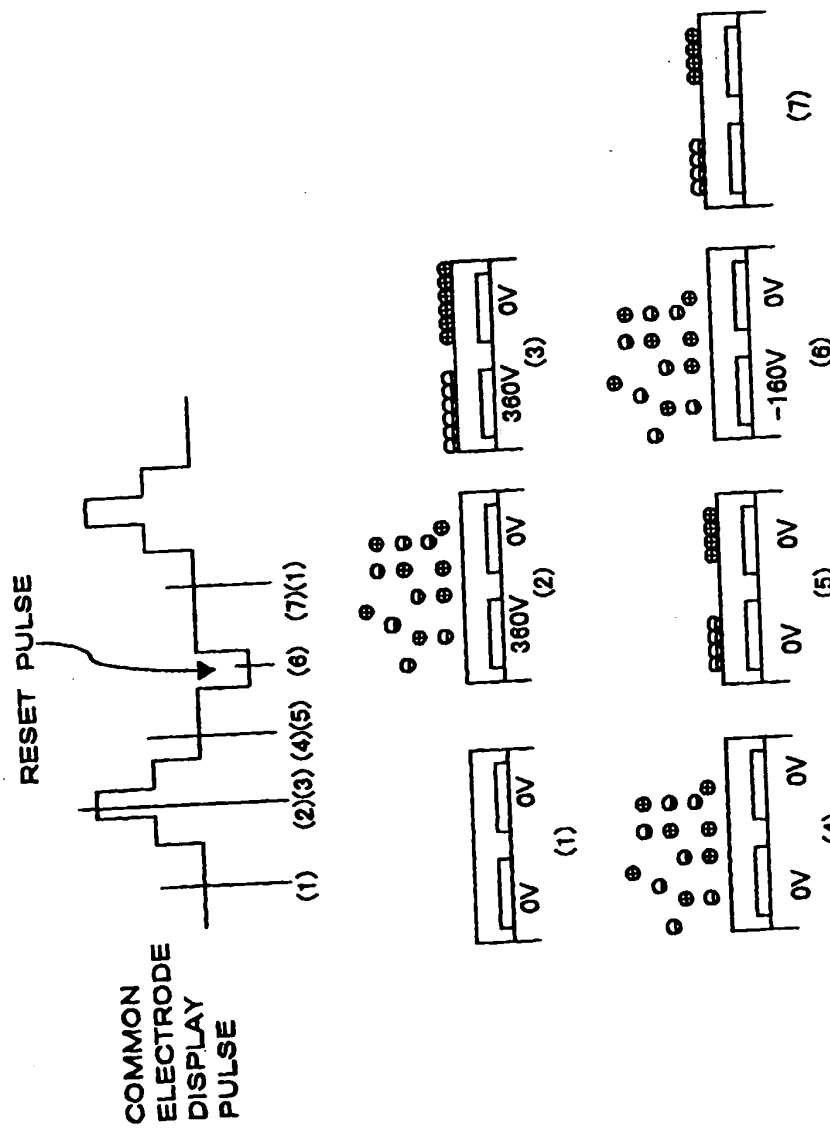
RESET PULSE
COMMON ELECTRODE DISPLAY PULSE
(1)
(2)(3)
(4)(5)
(6)
(7)(1)
0V
0V
(1)
360V
0V
(2)
360V
0V
(3)
0V
0V
(4)
0V
0V
(5)
-160V
0V
(6)
(7)

FIG. 11

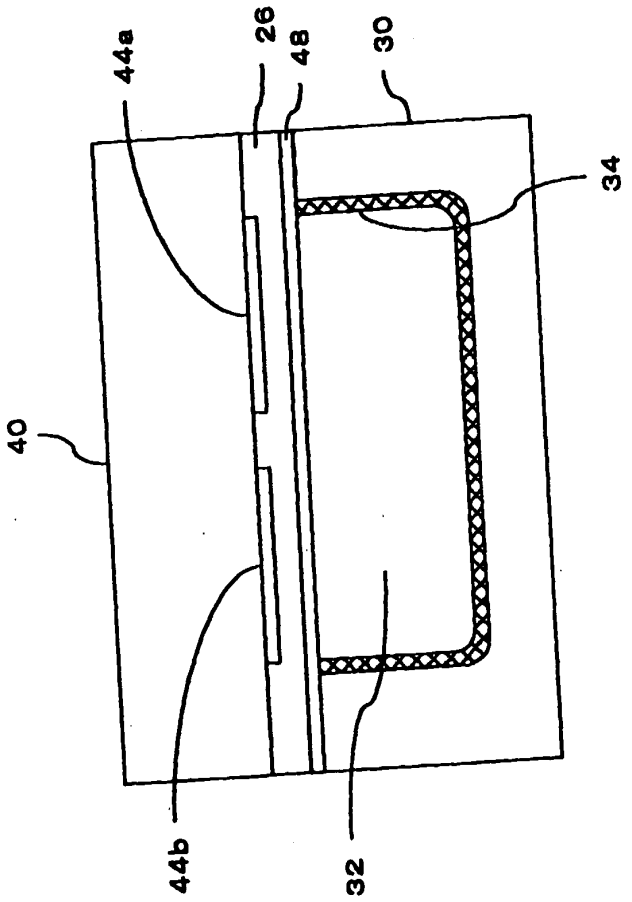

FIG. 12

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 10 5566

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 745 085 A (TOMIO ET AL) 28 April 1998 (1998-04-28)	1	G09G3/28
A	* abstract * * column 2, line 51 - column 3, line 20 * * column 10, line 24 - column 11, line 17; figures 1,7-9,14,15 *	2-5	
A	EP 0 653 740 A (FUJITSU LTD.) 17 May 1995 (1995-05-17) * abstract * * page 4, line 1 - line 49 * * page 7, line 53 - page 8, line 37 * * page 10, line 3 - line 43; figures 8,11 *	1-5	
A	EP 0 755 043 A (FUJITSU GENERAL LTD.) 22 January 1997 (1997-01-22) * abstract * * column 3, line 15 - column 5, line 25 * * column 6, line 42 - column 7, line 23; figure 4 *	1-5	
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	31 January 2000	O'Reilly, D

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